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EXAMINER	
HU, SHOUXIANG	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,811	GRAETTINGER ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *66-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *66-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 66-77 are objected to because of the following informalities and/or defects:

In claim 66, the terms of "an upper circuit element" and "a lower circuit element" recited in line 5 should read as: --said upper circuit element-- and –said lower circuit element--, respectively.

Furthermore, in claim 66, the term of "around at least one gate" should read as: --covering at least one gate--, since what under the gate is a gate dielectric layer; and the term of "conductive electrical connector" should read as: --electrical connector--, or –conductive connector--.

In claim 72, the terms of "a capacitor" and "a transistor" recited in line 6 should read as: --said capacitor-- and –said transistor—respectively.

In claims 74, and 76, the term of "surrounding" should read as: --covering--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 66-77 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 66-77 fail to clearly define the key subject matters of the method in the instant invention that the method comprises the steps of: forming the silicon nitride barrier liner on the inner sidewalls of a contact opening in an insulating interlayer; and then forming the conductive connector or plug inside the contact opening. What recited in these rejected claims, especially the limitations in claims 66 and 72, such as "forming a silicon nitride barrier liner around a conductive electrical connect" in claim 66 and "surrounding sidewalls of the first barrier layer with a second barrier" in claim 72, may imply that the silicon nitride barrier liner is formed after the formation of the conductive connector or plug, which is not readable on the specification and drawings of the instant invention.

In addition, claims 66 and 72 recite the term of "corrosive effects" or "corrosive aspects", but both fail to clearly define what is the corrosive effects or aspects. According to the original disclosure, it is not the upper circuit element (or the high dielectric constant dielectric or the capacitor) that is corrosive to the conductive connector (or plug). It is the required annealing in oxygen for the high dielectric constant dielectric that would adversely cause oxidation of the plug.

4. Claims 72-77 are further rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap

between the elements. See MPEP § 2172.01. The omitted elements are: the second barrier is formed with silicon nitride, as the disclosure does not identify any other insulating material that can also protecte the plug in the instant invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 66, 68 and 70-71, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartner et al. ("Hartner"; WO 98/15013; also see US 6,043,529 for its English translation; both are in record) in view of Juengling (US 5,700,706)

Hartner discloses a method for protecting conductive elements (such as plugs) from potential adverse oxidation during the annealing of a high dielectric constant layer (6) in a capacitor (see Fig. 2, col. 23, lines 63-67, and col. 1, line 30, through col. 2, line 17, in US 6,043,529), comprising the steps of: forming a gate (13); forming a silicon nitride barrier liner (16) covering the inner sidewalls of a contact opening in a dielectric interlayer (2); and forming conductive connector(s) or plug(s) (1) inside the silicon nitride barrier liner (16), wherein the conductive connect(s) or plug(s) electrically connect(s) the

capacitor (5-6; an upper circuit element) to a transistor active region (9; a lower circuit element).

Although Hartner does not expressly disclose that the method can further comprise the step of forming an insulating barrier liner covering the gate and in contacts with the a silicon nitride barrier liner, one of ordinary skill in the art would readily recognize that the gate can be preferably covered by an insulating barrier liner for better protection to the gate and for better alignment among the gate, channel and source/drain regions, and that the liner for the gate and the liner for the plug can be in contact for reducing size, as both evidenced in Juengling (see the silicon nitride gate liner 24 and silicon nitride plug liner 54 in Figs. 2 and 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make a semiconductor device of Hartner with the method further comprising the step of forming a silicon nitride gate liner (the insulating barrier liner) in contact with the silicon nitride (plug) barrier liner, as taught in Juengling, so that a method for making a semiconductor device with better protection to the gate and better structure alignment and with reduced size would be achieved.

Regarding claim 70, the capacitor dielectric layer in Hartner can be formed with a ferroelectric material (see col. 1, lines 61-67), which would naturally have a dielectric constant greater than about 10.

7. Claim 67, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a)

as being unpatentable over Hartner in view of Juengling, as applied to claims 66, 68 and 70-71 above, and further in view of Cho et al. ("Cho"; US 5,346,844; of record).

The disclosure of Hartner and Juengling are discussed as applied to claims 66, 68 and 70-71 above.

Although Hartner and Juengling do not expressly disclose that portions of the gate can be in contact with the silicon nitride (plug) barrier liner, one of ordinary skill in the art would readily recognize that such a silicon nitride (plug) barrier liner can be in contact with portions of the gate for further reducing the device size, as evidenced in the prior art such as Cho (see the gate electrode (18) in direct contact with the silicon nitride plug liner (40) in Fig. 3A)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the above collectively taught method to make a semiconductor device with portions of the gate being in contact with the silicon nitride (plug) barrier liner, as taught in Cho, so that a method for making a semiconductor device with better protection to the gate and better structure alignment and with reduced size would be achieved.

8. Claim 69, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartner in view of Juengling, as applied to claims 66, 68 and 70-71 above, and further in view of Sun et al. ("Sun"; US 4,926,237).

The disclosure of Hartner and Juengling are discussed as applied to claims 66, 68 and 70-71 above.

Hartner further teaches to form a conductive barrier liner (3) on top of the electrical connector (plug).

Although Hartner and Juengling do not expressly disclose that the method can further comprise the step of forming a conductive barrier liner between the silicon nitride barrier liner and the electrical connector (plug), Sun teaches that an electrical plug (28) formed inside a dielectric layer (16, including silicon nitride, see col. 3, lines 12-14) can desirably have a conductive diffusion barrier liner (22, 26, and/or 24) disposed therebetween, i.e., forming the conductive diffusion barrier prior to the formation of the plug, which also naturally forms a conductive barrier liner at the bottom of the electrical plug, for providing better protection to the electrical plug.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporating the step of forming the conductive barrier liner of Sun into the above collectively taught method, so that a method for making a semiconductor device with better protection to the electrical plug would be obtained.

9. Claims 72-76, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartner et al. ("Hartner"; WO 98/15013; also see US 6,043,529 for its English translation; both are in record) in view of Sun et al. ("Sun"; US 4,926,237).

Hartner discloses a method for protecting conductive elements (such as plugs) from potential adverse oxidation during the annealing of a high dielectric constant layer (6) in a capacitor (see Fig. 2, col. 23, lines 63-67, and col. 1, line 30, through col. 2, line 17, in US 6,043,529), comprising the steps of: forming a gate (13); forming a second barrier (16, silicon nitride barrier liner) covering the inner sidewalls of a contact opening in a dielectric interlayer (2); and forming a conductive contact plug (1) inside the silicon nitride barrier liner (16); and forming a capping barrier(3; readable as the third barrier recited in claim 73), wherein the conductive contact plug electrically connects the capacitor (5-6; an upper circuit element) to a transistor active region (9; a lower circuit element).

Although Hartner does not expressly disclose that the method can further comprise the step of forming a first barrier (a conductive barrier liner) between the second barrier (the silicon nitride barrier liner) and the contact plug, Sun teaches that a contact plug (28) formed inside a dielectric layer (16, including silicon nitride, see col. 3, lines 12-14) can desirably have a first barrier (a conductive diffusion barrier liner, 22, 26, and/or 24) disposed therebetween, i.e., forming the conductive diffusion barrier prior to the formation of the plug, which also naturally forms a conductive barrier liner at the bottom of the electrical plug, for providing better protection to the electrical plug.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporating the step of forming the conductive barrier liner of Sun into the method of Hartner, so that a method for making a semiconductor device with better protection to the contact plug would be obtained. And, with the first

barrier (the conductive diffusion barrier) being formed prior to the formation of the plug in the above collectively taught device, the first barrier would be naturally formed between the second barrier and the plug; and the bottom barrier would be naturally formed between the plug and the transistor active area in the substrate.

Regarding claim 75, it is noted that one of ordinary skill in the art would readily recognize that the gate (i.e., a bit or word line) can be preferably covered by an insulating layer including a sidewall portion and a cap portion for better protection to the gate and for better alignment among the gate, channel and source/drain regions, as evidenced in the prior art such as Juengling (see the silicon nitride gate liner 24 in Figs. 2 and 6).

10. Claim 77, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartner in view of Sun, as applied to claims 72-76 above, and further in view of Cho et al. ("Cho"; US 5,346,844; of record).

The disclosure of Hartner and Sun are discussed as applied to claims 72-76 above.

Although Hartner and Sun do not expressly disclose that portions of the gate (i.e., a bit or word line) can be in contact with the silicon nitride (plug) barrier liner (i.e., the second barrier), one of ordinary skill in the art would readily recognize that such a silicon nitride (plug) barrier liner can be in contact with portions of the gate for further reducing the device size, as evidenced in the prior art such as Cho (see the gate

electrode (18) in direct contact with the silicon nitride plug liner (40) in Fig. 3A, wherein the method for making the device in Cho further including the step of forming an insulating layer (20) including a sidewall portion and a cap portion covering the gate electrode (18))

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the above collectively taught method to make a semiconductor device with portions of the gate being in contact with the silicon nitride (plug) barrier liner being in contact with silicon nitride (plug) barrier liner, as taught in Cho, so that a method form making a semiconductor device with reduced size would be achieved.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703) 306-5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SH
May 30, 2003

Shouxiang Hu
Patent Examiner
TC2800